Please amend the present application as follows:

Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("———"), as is applicable:

1-17. (Canceled)

18. (Currently Amended) A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising:

forming trenches in a semiconductor-on-insulator substrate;

conformally coating ~~the semiconductor-on-insulator substrate~~ sidewalls of the trenches with an oxide;

filling the coated trenches with polysilicon, wherein electrodes are derived from the polysilicon;

forming release openings and removing the polysilicon and at least a portion of the semiconductor-on-silicon substrate; and

removing the conformally coated oxide and an oxide of the semiconductor-on-insulator substrate, wherein a capacitive gap is formed, wherein a resonating element of one of the capacitive resonators is released.

19. (Currently Amended) The method of claim 18, further including:

growing and patterning an insulator oxide, wherein the insulator oxide provides isolation between the semiconductor-on-insulator substrate and wire-bonding pads;

depositing and patterning nitride, wherein the nitride provides protection for the insulator oxide disposed on the pads;

growing and removing a surface treatment oxide, wherein the surface treatment oxide enables the reduction of the roughness of sidewalls of the resonating element;

depositing polysilicon to form the wirebonding pads for drive and sense electrodes;

metallizing the pads; and

wherein removing the polysilicon includes patterning the polysilicon inside the trenches.

20. (Original) The method of claim 18, wherein the forming release openings comprises anisotropically etching to an oxide layer of the semiconductor-on-substrate, such that the undercut of the resonating element is facilitated.

21. (Original) The method of claim 18, wherein the filling includes one of filling the trenches with doped LPCVD polysilicon such that the electrodes are formed vertically and depositing and patterning doped LPCVD polysilicon.

22. (Original) The method of claim 18, wherein the forming trenches includes one of deep reactive ion etching and regular reactive ion etching to an oxide layer of the semiconductor-on-insulator substrate.

23. (Original) The method of claim 18, wherein the conformally coating includes depositing a LPCVD high-temperature oxide of approximately less than 100 nanometers.

24. (Original) The method of claim 18, wherein the conformally coating is scalable to correspond to a desired thickness of a lateral gap spacing for the capacitive resonator.

25. (Original) The method of claim 18, wherein the removing comprises an anisotropic plasma etching such that at least a portion of the oxide remains on sidewalls of the resonating element.

26. (Original) The method of claim 18, wherein the releasing comprises exposing the semiconductor-on-insulator substrate to a solution comprising HF:H20 to release the resonating element from a handle layer and the electrodes.

27. (Original) The method of claim 18, wherein the forming trenches includes etching high-aspect ratio trenches.

28. (Original) The method of claim 18, wherein the removing includes forming a gap between the resonating element and the polysilicon in a self-aligned manner.

29-35. (Canceled)

36. (Previously presented) The method of claim 18, wherein the removing is performed to form a plurality of capacitive gaps and release a plurality of resonating elements, each of the plurality of resonating elements electrically isolated from each other.

37. (New) A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising:

forming trenches in a semiconductor-on-insulator substrate;

conformally coating the sidewalls of the trenches with an oxide;

filling the coated trenches with polysilicon, wherein electrodes are derived from the polysilicon;

forming release openings and removing the polysilicon and at least a portion of the semiconductor-on-silicon substrate without isotropic etching of the polysilicon or semiconductor portion of the semiconductor-on-silicon substrate; and

removing the conformally coated oxide and an oxide of the semiconductor-on-insulator substrate, wherein a capacitive gap is formed, wherein a resonating element of one of the capacitive resonators is released.

38. (New) The method of claim 37, further including:

growing and patterning an insulator oxide, wherein the insulator oxide provides isolation between the semiconductor-on-insulator substrate and wire-bonding pads;

depositing and patterning nitride, wherein the nitride provides protection for the insulator oxide disposed on the pads;

growing and removing a surface treatment oxide, wherein the surface treatment oxide enables the reduction of the roughness of sidewalls of the resonating element;

depositing polysilicon to form the wirebonding pads for drive and sense electrodes;

metallizing the pads; and

wherein removing the polysilicon includes patterning the polysilicon inside the trenches.

39. (New) The method of claim 37, wherein the forming release openings comprises anisotropically etching to an oxide layer of the semiconductor-on-substrate, such that the undercut of the resonating element is facilitated.

40. (New) The method of claim 37, wherein the filling includes one of filling the trenches with doped LPCVD polysilicon such that the electrodes are formed vertically and depositing and patterning doped LPCVD polysilicon.

41. (New) The method of claim 37, wherein the forming trenches includes one of deep reactive ion etching and regular reactive ion etching to an oxide layer of the semiconductor-on-insulator substrate.

42. (New) The method of claim 37, wherein the conformally coating includes depositing a LPCVD high-temperature oxide of approximately less than 100 nanometers.

43. (New) The method of claim 37, wherein the conformally coating is scalable to correspond to a desired thickness of a lateral gap spacing for the capacitive resonator.

44. (New) The method of claim 37, wherein the removing comprises an anisotropic plasma etching such that at least a portion of the oxide remains on sidewalls of the resonating element.

45. (New) The method of claim 37, wherein the releasing comprises exposing the semiconductor-on-insulator substrate to a solution comprising HF:H20 to release the resonating element from a handle layer and the electrodes.

46. (New) The method of claim 37, wherein the forming trenches includes etching high-aspect ratio trenches.

47. (New) The method of claim 37, further including conformally coating surfaces of the semiconductor-on-insulator substrate with the oxide associated with conformal coating.

48. (New) A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators having sharply defined boundaries, the method consisting of:

growing or depositing an oxide layer on a semiconductor-on-insulator substrate and patterning the oxide to the shape of the resonators;

forming trenches in the semiconductor-on-insulator substrate by using the oxide layer as a mask;

conformally coating sidewalls of the trenches with an oxide;

filling the coated trenches with polysilicon, wherein electrodes are derived from the polysilicon;

forming release openings and removing the polysilicon and at least a portion of the semiconductor-on-silicon substrate without isotropic etching of the polysilicon or semiconductor portion of the semiconductor-on-silicon substrate; and

forming a resonating element having sharply defined boundaries of one of the capacitive resonators by removing the conformally coated oxide and an oxide of the semiconductor-on-insulator substrate, wherein a capacitive gap is formed, wherein the resonating element is released.

49. (New) A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators having a height-to-width ratio of less than one, the method comprising:

forming trenches in a semiconductor-on-insulator substrate;

conformally coating sidewalls of the trenches with an oxide;

filling the coated trenches with polysilicon, wherein electrodes are derived from the polysilicon;

forming release openings and removing the polysilicon and at least a portion of the semiconductor-on-silicon substrate without isotropic etching of the polysilicon or semiconductor portion of the semiconductor-on-silicon substrate; and

forming a resonating element having a height-to-width ratio of less than one of the capacitive resonators by removing the conformally coated oxide and an oxide of the semiconductor-on-insulator substrate, wherein a capacitive gap is formed, wherein the resonating element is released.

50. (New) The method of claim 49, further including:

growing and patterning an insulator oxide, wherein the insulator oxide provides isolation between the semiconductor-on-insulator substrate and wire-bonding pads;

depositing and patterning nitride, wherein the nitride provides protection for the insulator oxide disposed on the pads;

growing and removing a surface treatment oxide, wherein the surface treatment oxide enables the reduction of the roughness of sidewalls of the resonating element;

depositing polysilicon to form the wirebonding pads for drive and sense electrodes;

metallizing the pads; and

wherein removing the polysilicon includes patterning the polysilicon inside the trenches.

51. (New) The method of claim 49, wherein the forming release openings comprises anisotropically etching to an oxide layer of the semiconductor-on-substrate, such that the undercut of the resonating element is facilitated.

52. (New) The method of claim 49, wherein the filling includes one of filling the trenches with doped LPCVD polysilicon such that the electrodes are formed vertically and depositing and patterning doped LPCVD polysilicon.

53. (New) The method of claim 49, wherein the forming trenches includes one of deep reactive ion etching and regular reactive ion etching to an oxide layer of the semiconductor-on-insulator substrate.

54. (New) The method of claim 49, wherein the conformally coating includes depositing a LPCVD high-temperature oxide of approximately less than 100 nanometers.

55. (New) The method of claim 49, wherein the conformally coating is scalable to correspond to a desired thickness of a lateral gap spacing for the capacitive resonator.

56. (New) The method of claim 49, wherein the removing comprises an anisotropic plasma etching such that at least a portion of the oxide remains on sidewalls of the resonating element.

57. (New) The method of claim 49, wherein the releasing comprises exposing the semiconductor-on-insulator substrate to a solution comprising HF:H20 to release the resonating element from a handle layer and the electrodes.

58. (New) the method of claim 49, further comprising conformally coating surfaces of the semiconductor-on-insulator substrate with the oxide associated with conformal coating.

59. (New) The method of claim 18, further including conformally coating surfaces of the semiconductor-on-insulator substrate with the oxide associated with conformal coating.